

# GA-F2A68HM-DS2

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APU\_VDDIO\_SUS=DDR15V

APU\_VTT\_SUS=DDRVTT

APU\_VDDP\_RUN=APU\_VDDR\_RUN=APU\_VDDP

+1.1V\_RUN=FCH\_VDD\_11\_RUN=VCC\_SB

+3.3V\_RUN=VCC3

+3.3V\_ALW=3VDUAL

GIGABYTE™

Title

COVER SHEET

Size

Custom

Document Number

GA-F2A68HM-DS2

Rev

1.01

Date:

Tuesday, October 28, 2014

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**Model Name:GA-F2A68HM-DS2**


## Component value change history

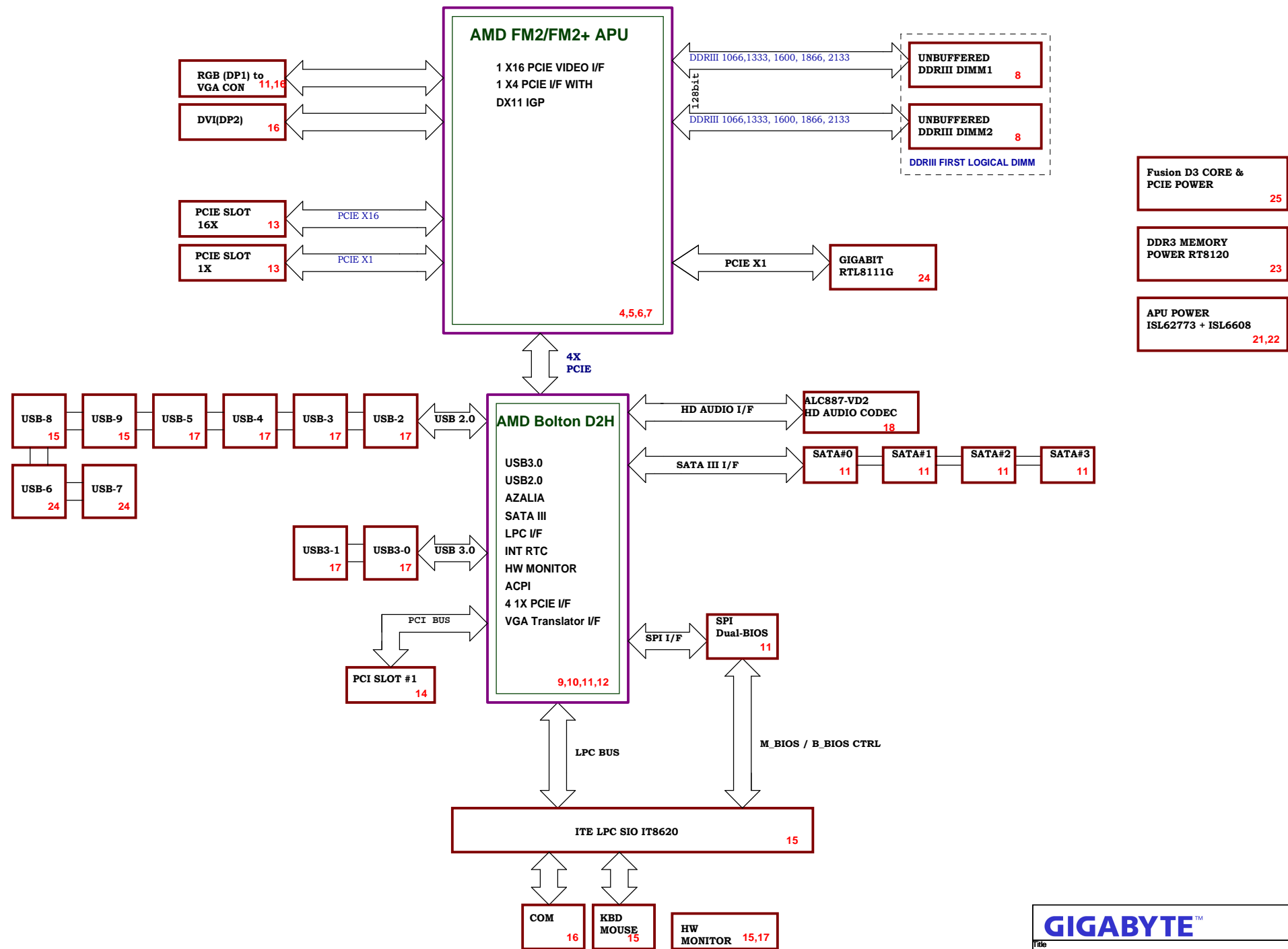
**Version: 1.01**  
9MF278MS2-00  
P-Code: U14076-0

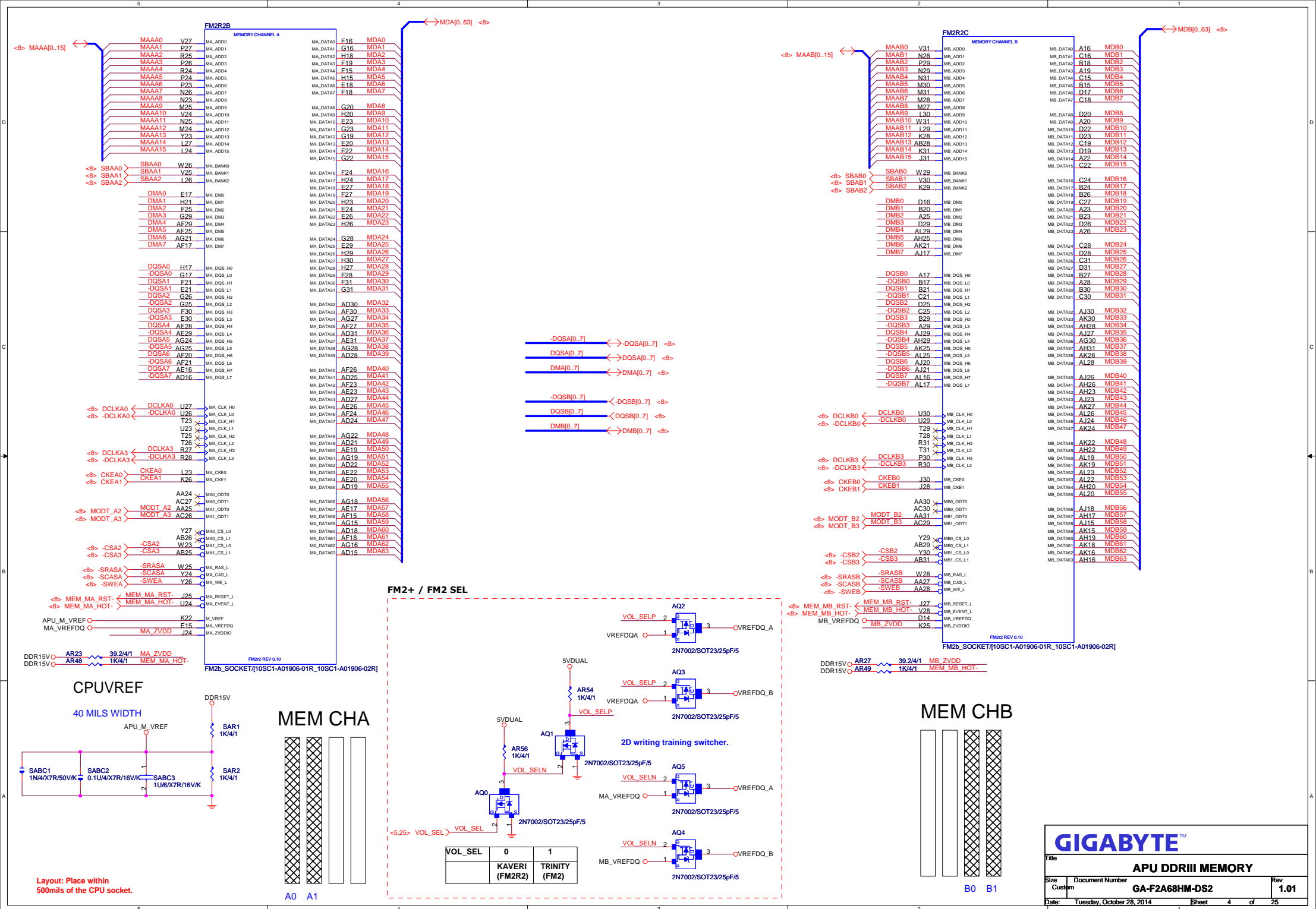
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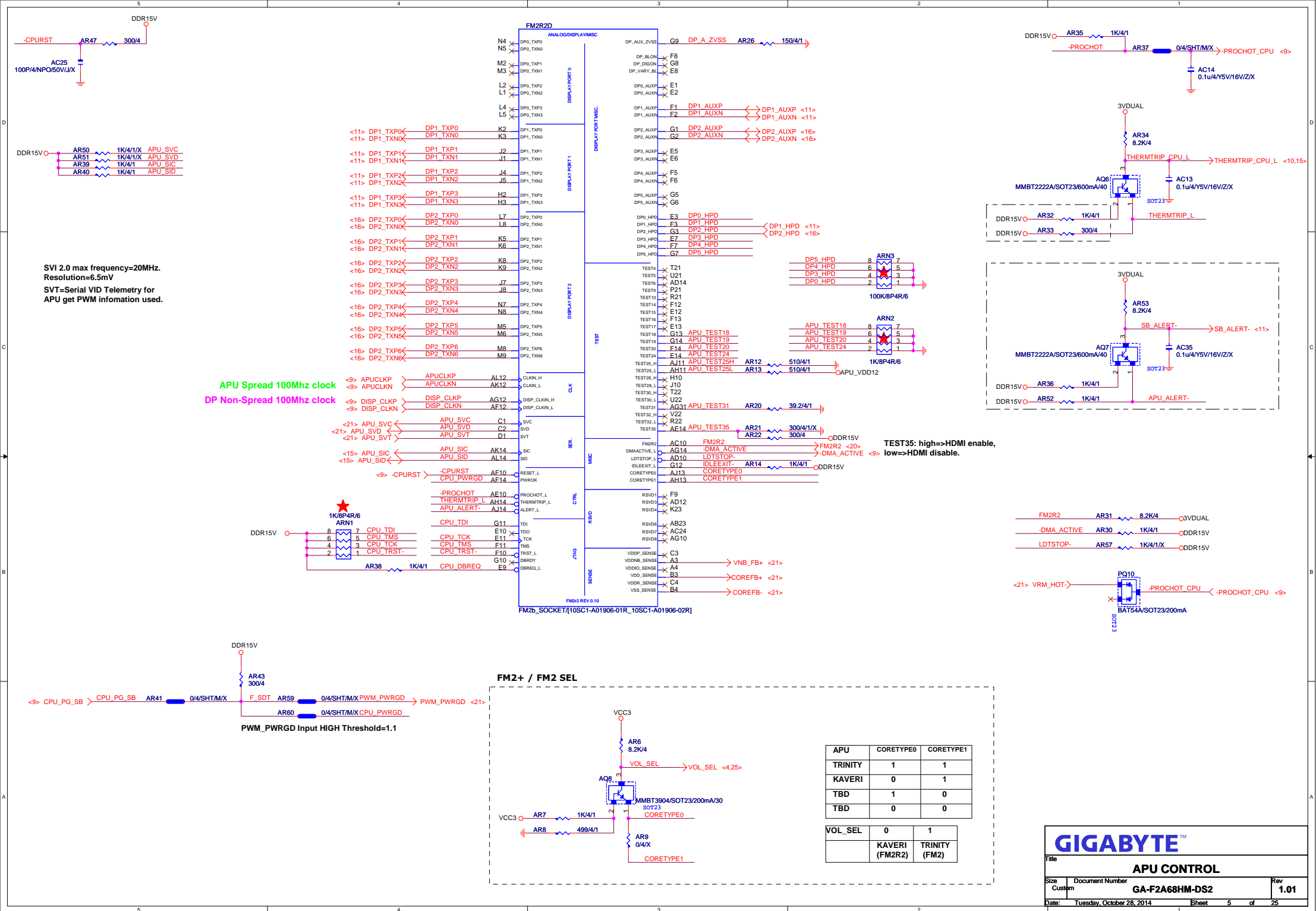
### Circuit or PCB layout change for next version

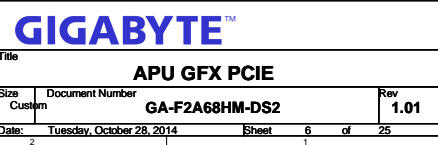
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<b>Title</b>				
<b>BOM &amp; PCB HISTORY</b>				
<b>Size</b>	<b>Document Number</b>			<b>Rev</b>
Custom	<b>GA-F2A68HM-DS2</b>			<b>1.01</b>
<b>Date:</b>	Tuesday, October 28, 2014		<b>Sheet</b>	2 of 25

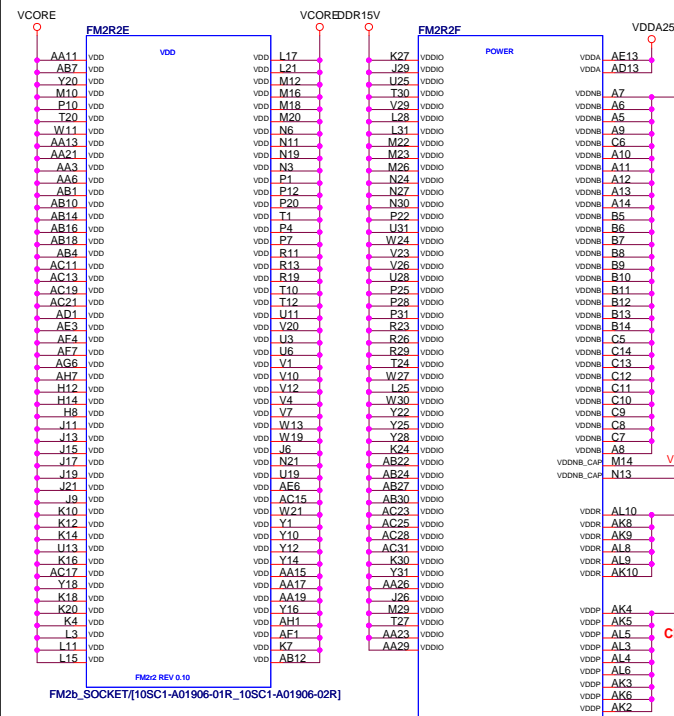




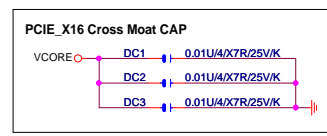
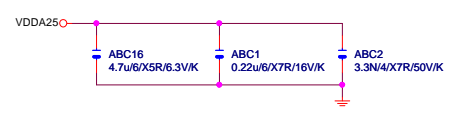




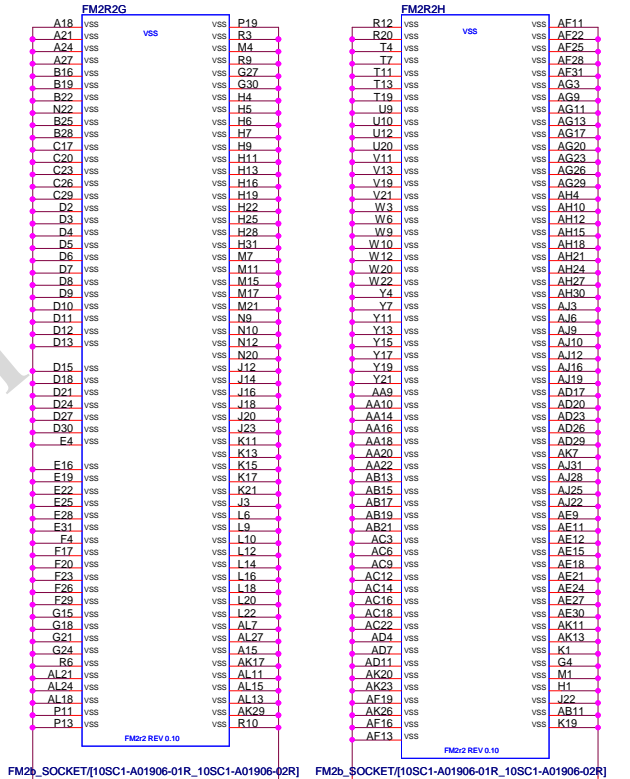
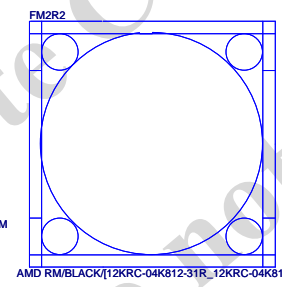
DDR15V=1.25V/1.35V/1.5V(DDR3)



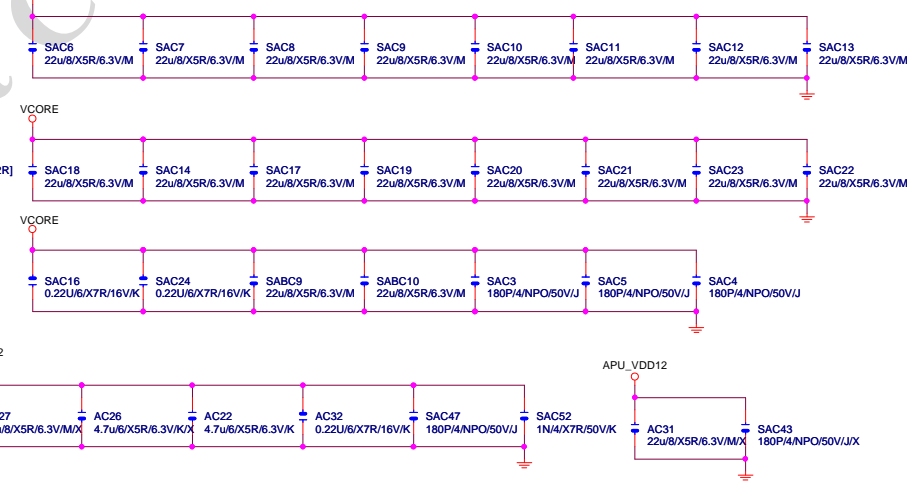
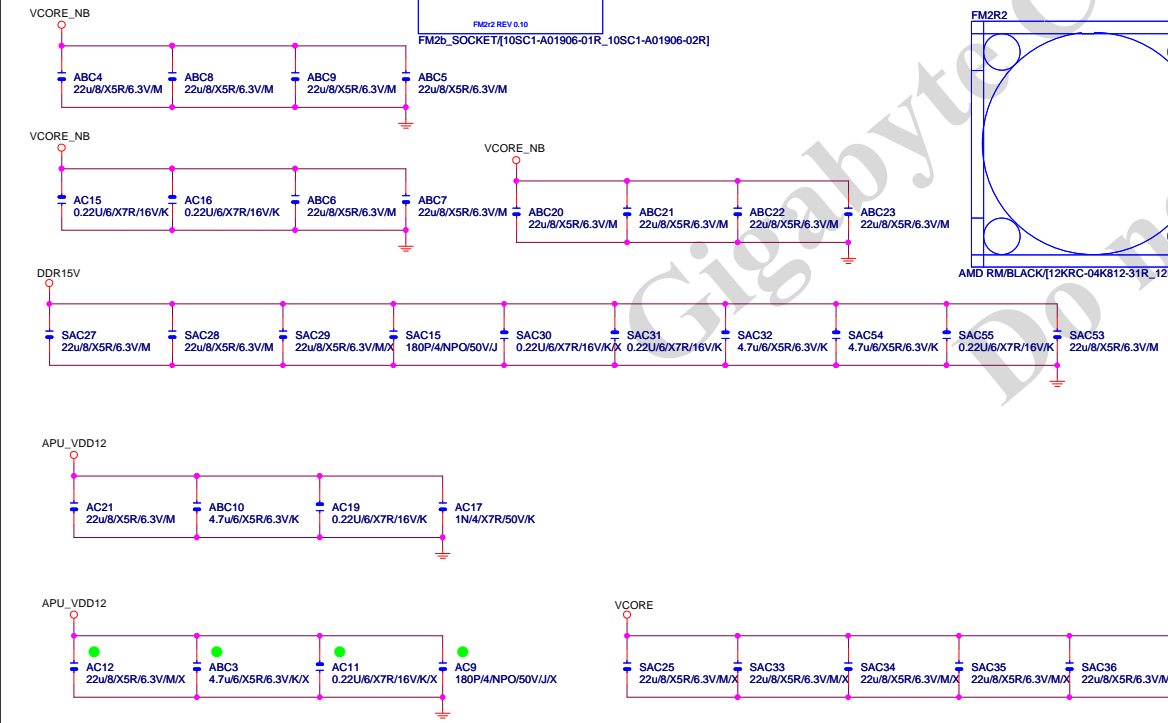
GND:232 pin,  
VCORE:99 pin,  
VCORE\_NB: 30 pin,  
DDR15V:49 pin,  
VDDP:9 pin, VDDR:9  
pin, VDDA25:2 pin,  
VDDNB\_CAP:2  
pin, Total:430 pin.



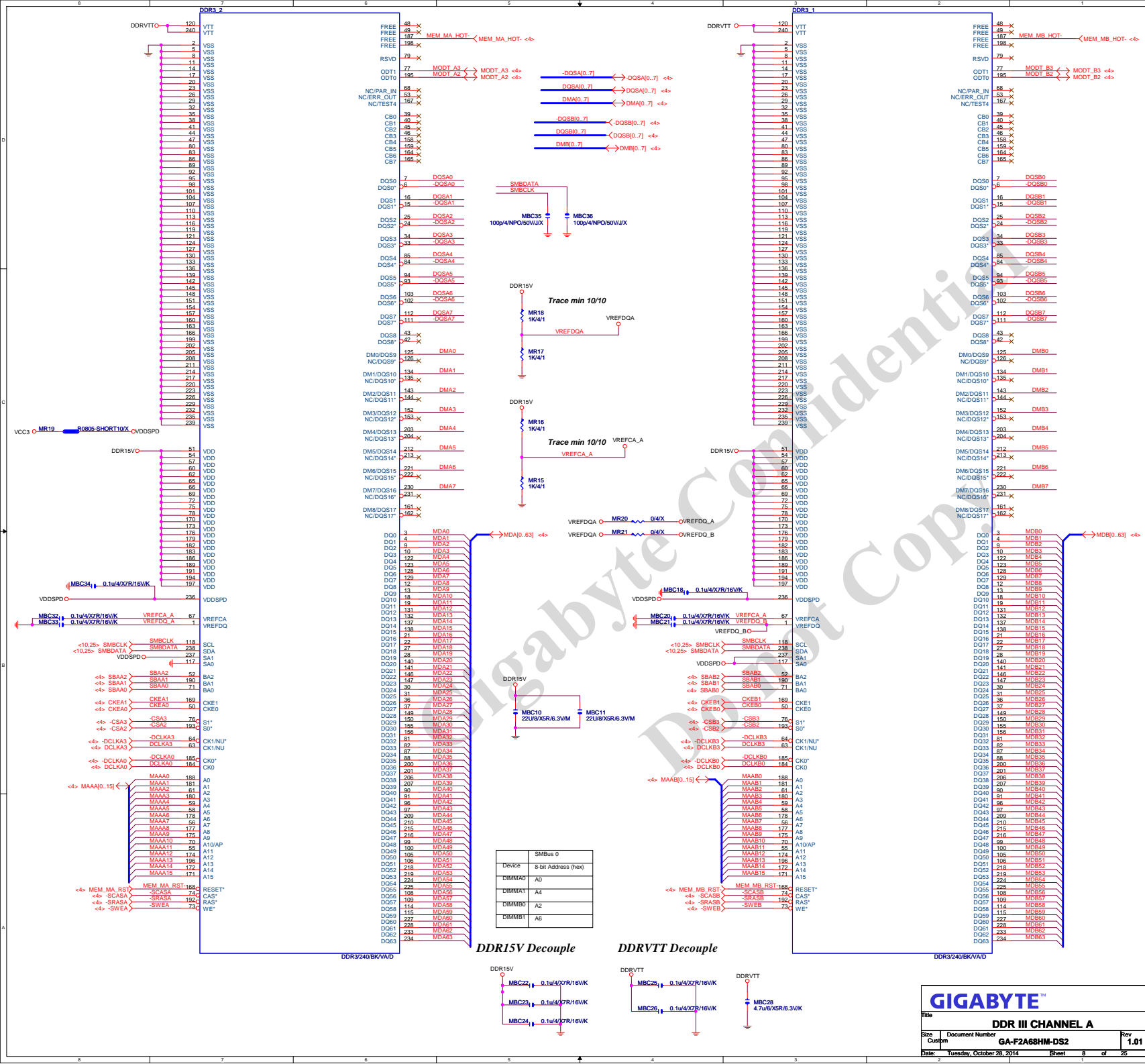
Place close N13, M14 pin inside  
the backplate cavity opening.



BOTTOM SIDE



GIGABYTE™			
Title APU POWER & GND			
Size Custom	Document Number GA-F2A68HM-DS2	Rev 1.01	
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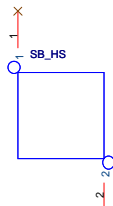




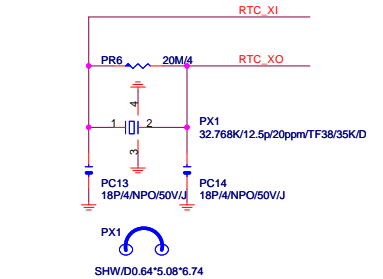


PLACE THESE PCIE AC COUPLING  
CAPS CLOSE TO SB850

### S.B HEATSINK

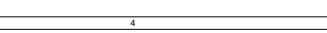
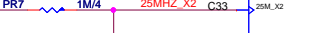
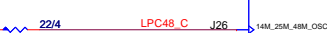
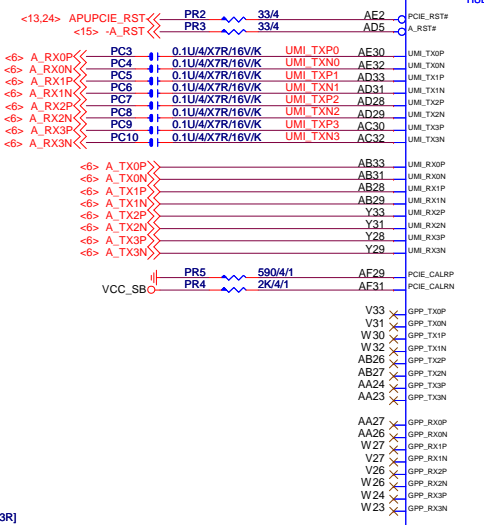


SB\_HS[12SP2-SA0301-11R\_12SP2-SA0301-12R\_12SP2-SA0301-13R]

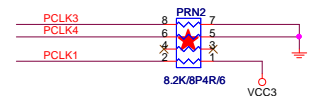
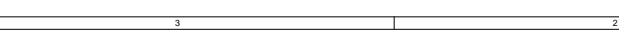
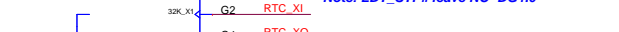
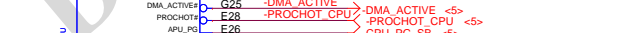
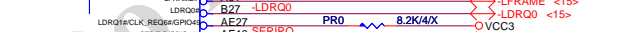
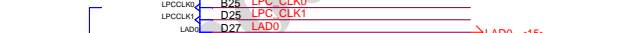
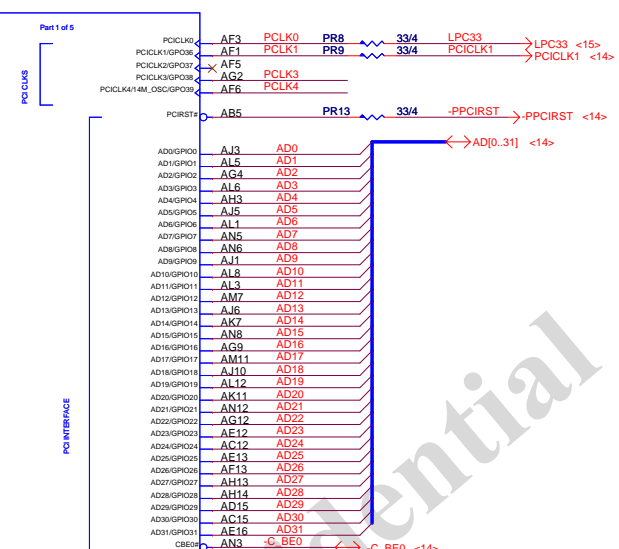


SHW/D0.64\*5.08\*6.74

### For APU PCI\_E devices.



### HUDSON-2



**PCLK3**  
PULL HIGH  
PULL LOW

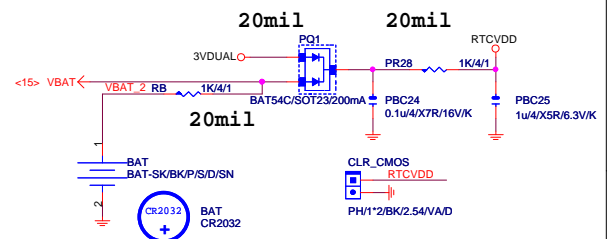
**USE**  
DEBUG STRAPS  
IGNORE DEBUG STRAPS  
DEFAULT

CLKGEN Mode: Only for integrated clock mode.



**LPC\_CLK0**  
PULL HIGH  
PULL LOW

**LPC\_CLK1**  
IMC ENABLED  
IMC DISABLED  
CLKGEN ENABLED  
CLKGEN DISABLED  
DEFAULT



CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

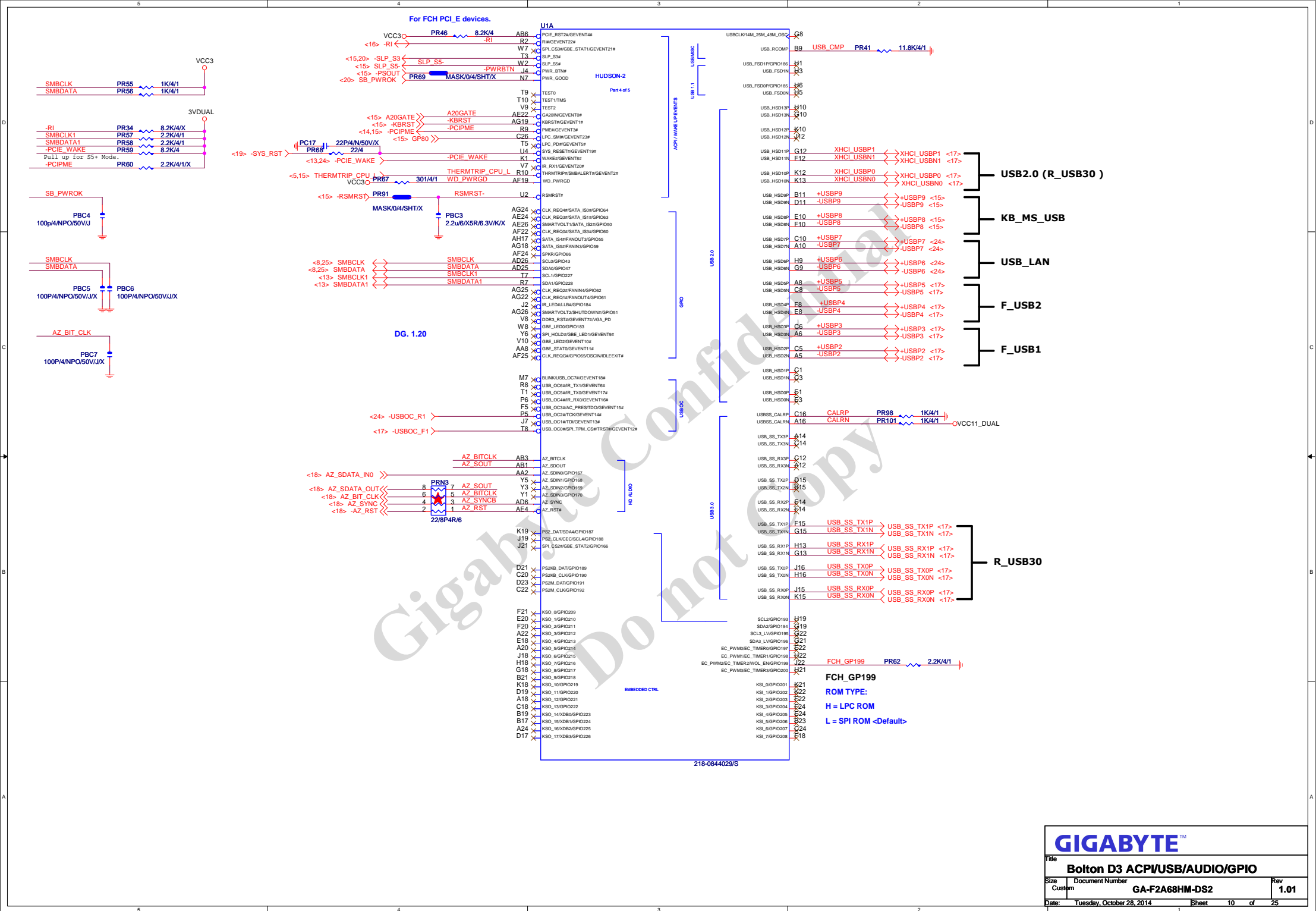
NOT ADD ICT FOR RTCVDD PIN

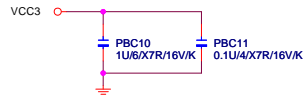
**GIGABYTE**  
Title  
**Bolton D3 PCIE/PCI/CPU/LPC**  
Size Custom  
Document Number  
**GA-F2A68HM-DS2**  
Date: Tuesday, October 28, 2014  
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Rev  
**1.01**



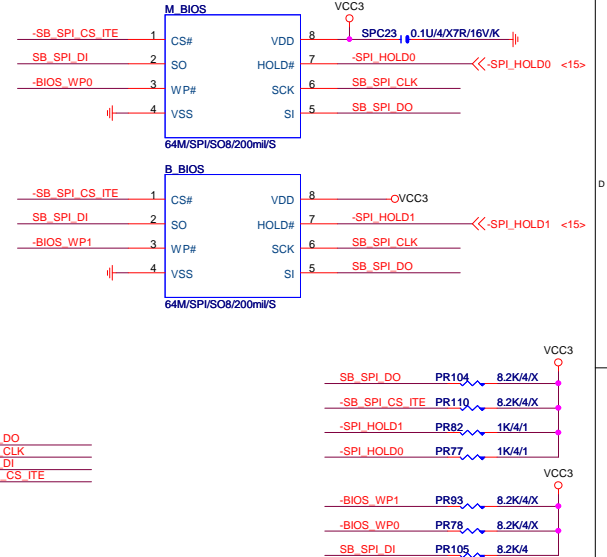
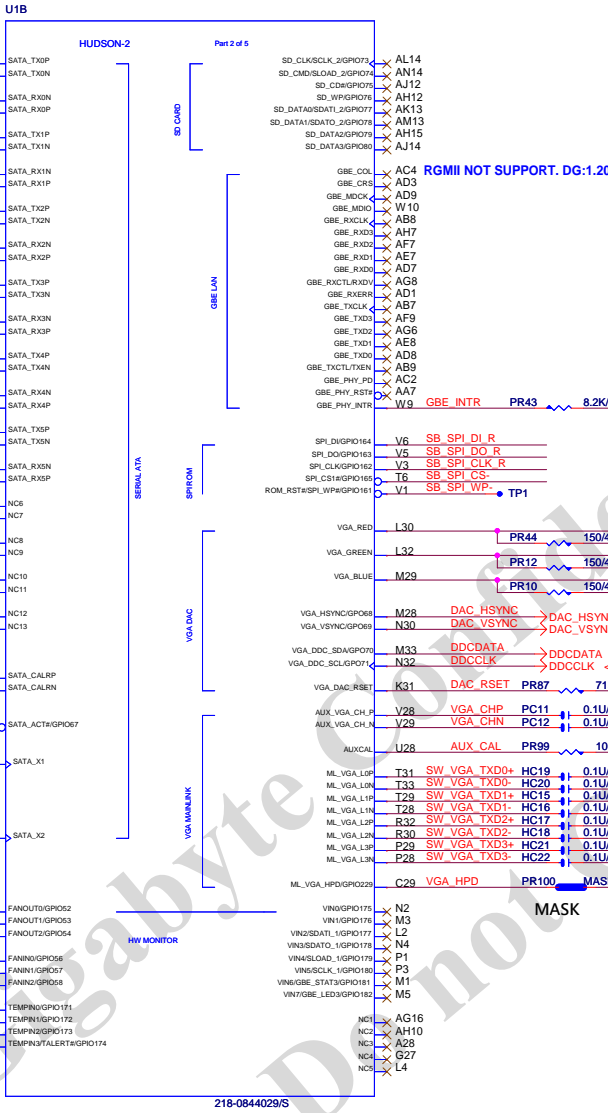
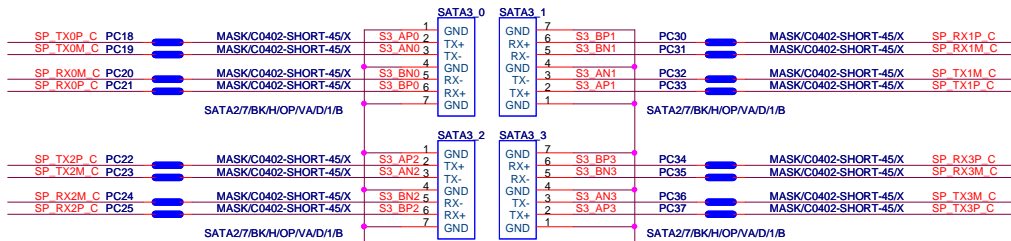
Pull down for S5+ Mode





SATA 6~7 for Hudson D4.

PLACE SATA\_CAL RES VERY CLOSE TO BALL OF U1



**GIGABYTE™**

TitleBolton D3 SATA/HWM/SPI

SizeCustomDocument NumberGA-F2A68HM-DS2Rev1.01

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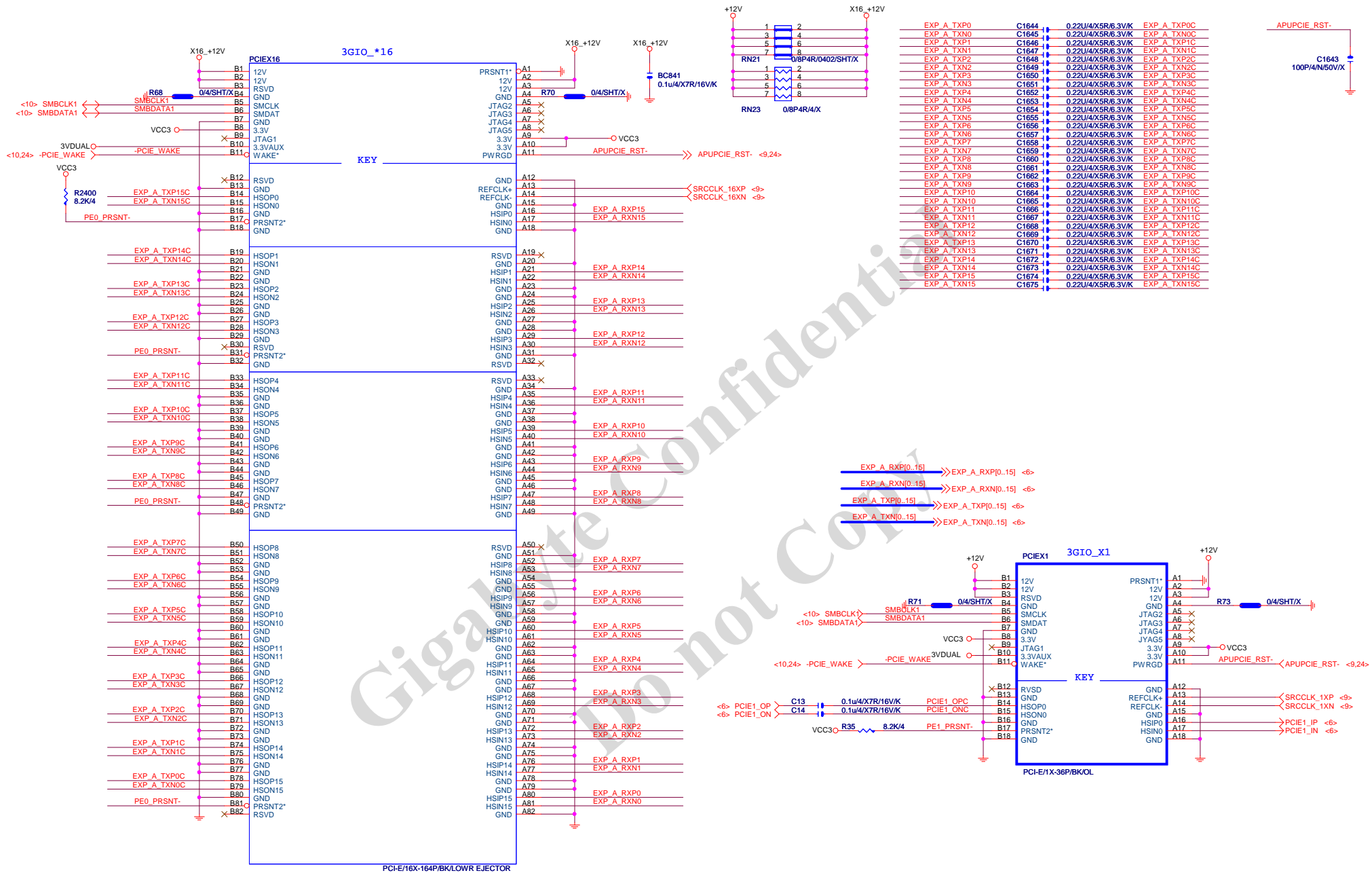
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

Hudson 3/4 does not support an RGMII/MII interface.

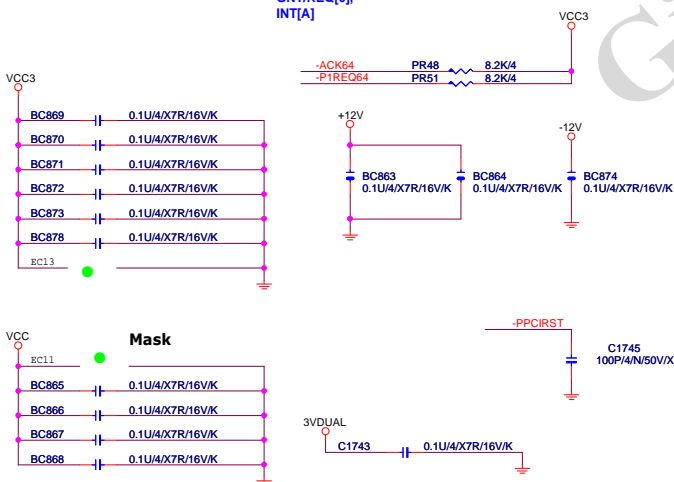
218-0844029/S

**GIGABYTE**

Title			
Bolton D3 POWER & GND			
Size	Document Number	Rev	
Custom	GA-F2A68HM-DS2	1.01	
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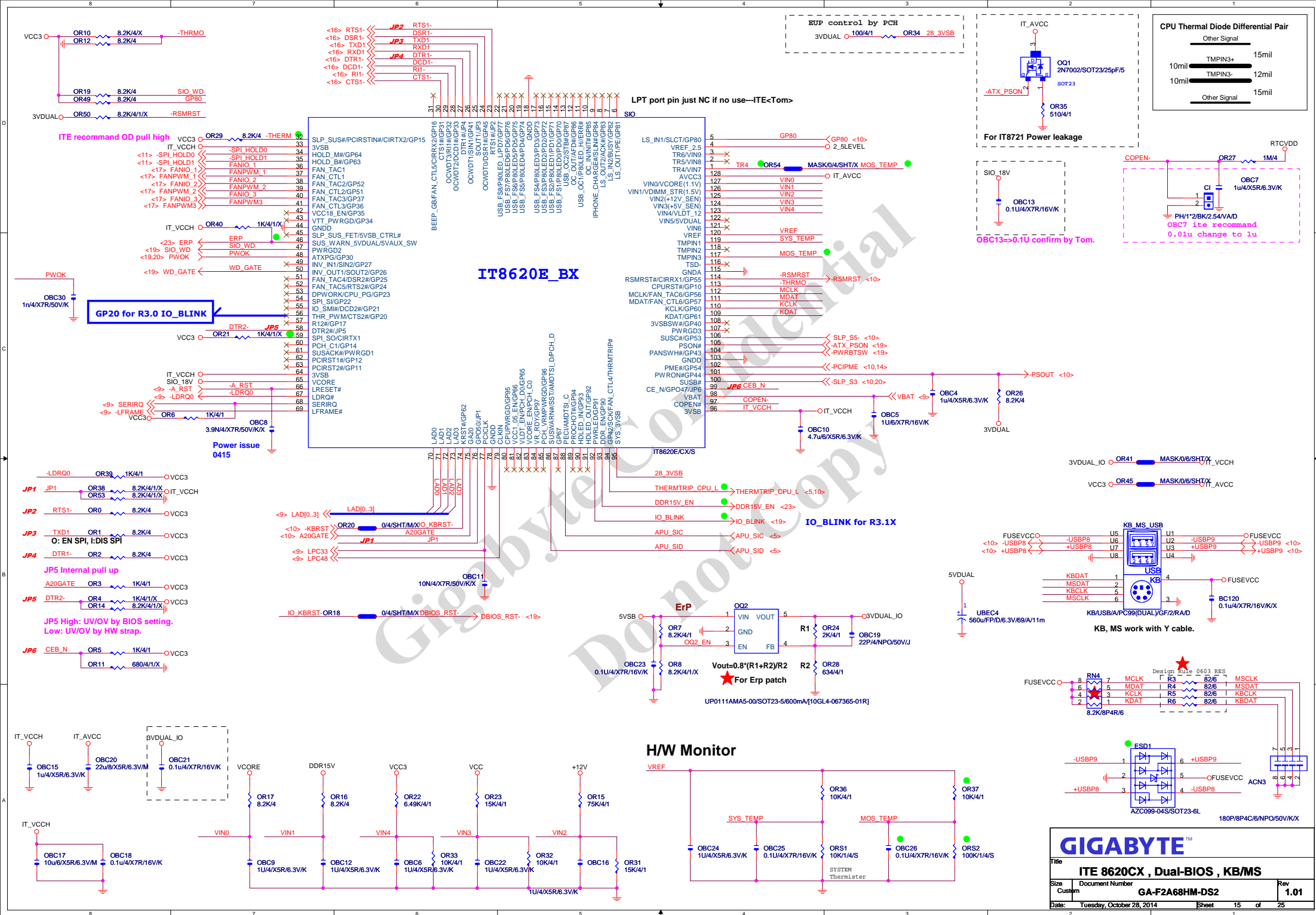


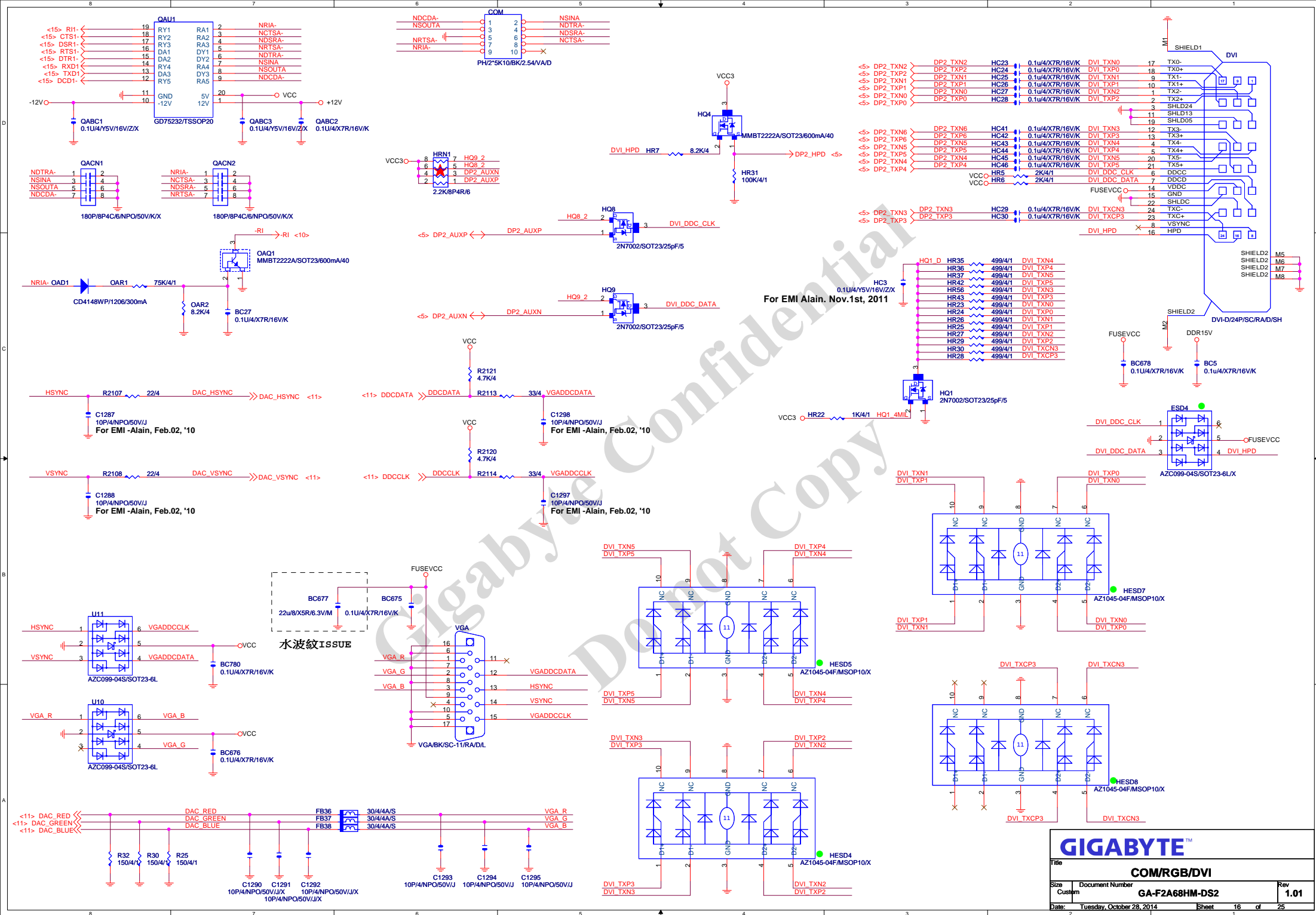
<9> AD[0..31]  $\longleftrightarrow$  AD[0..31]



Title			
PCI SLOT			
Size	Document Number	Rev	
Custom	GA-F2A68HM-DS2	1.01	
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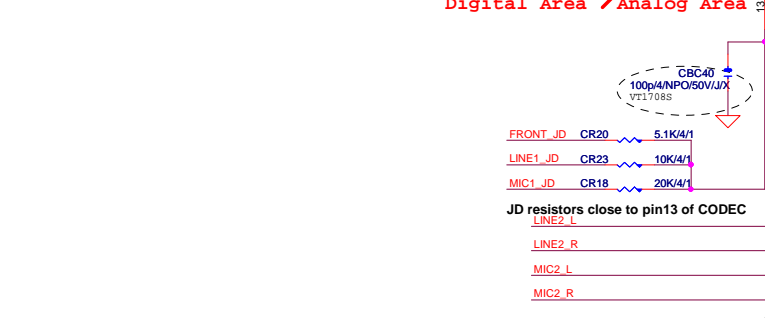
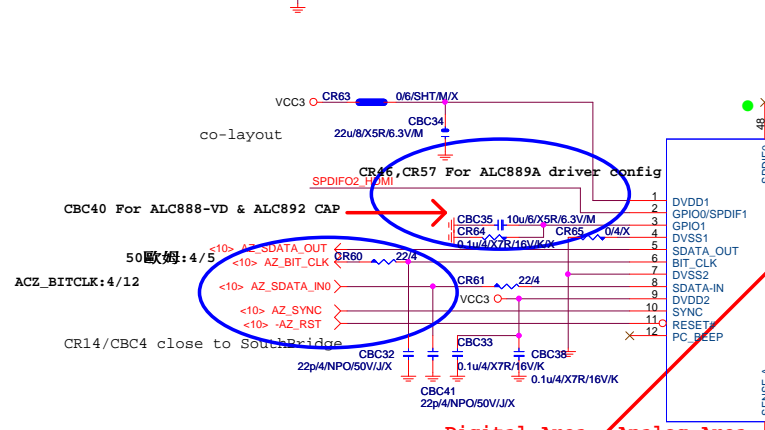
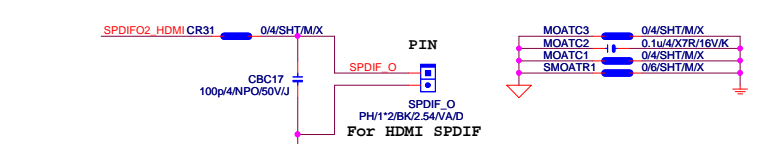








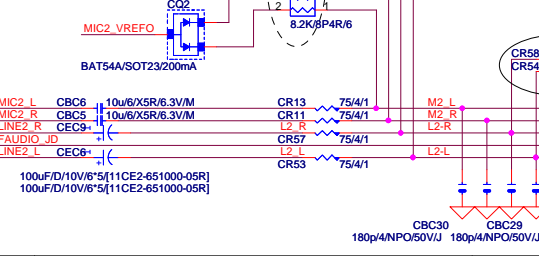
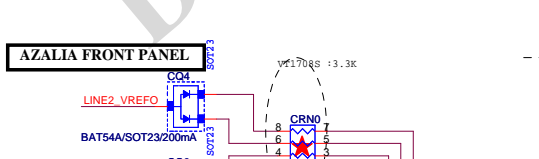
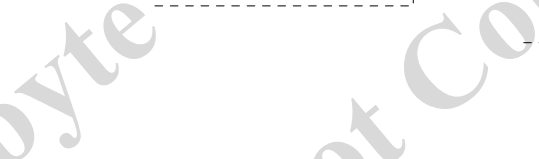
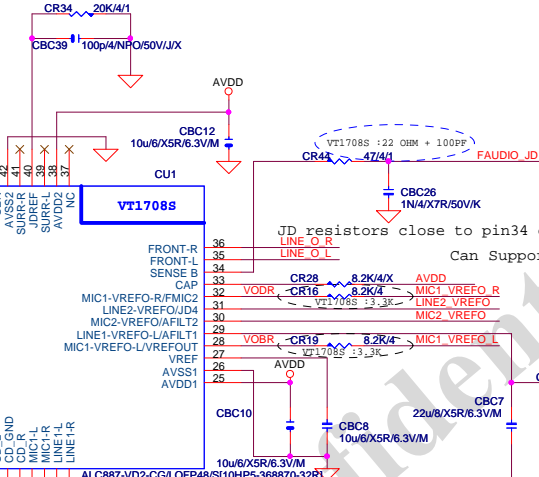
SPDIF\_OUT



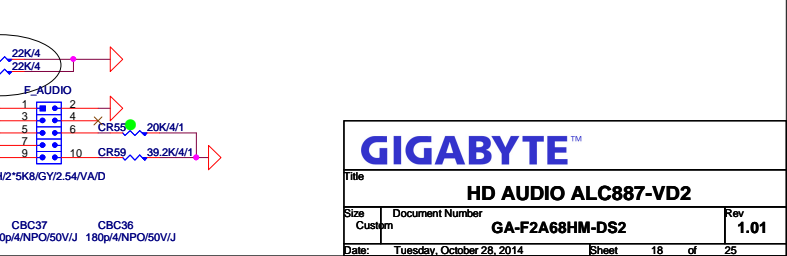
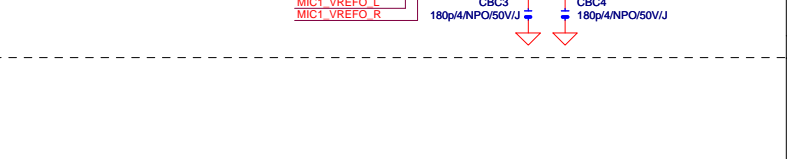
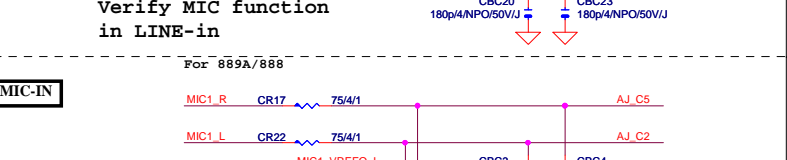
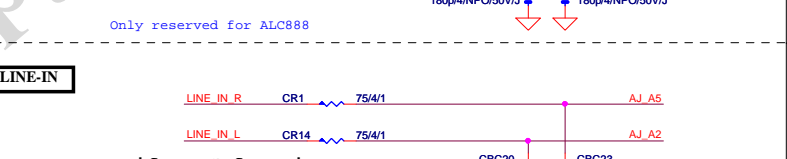
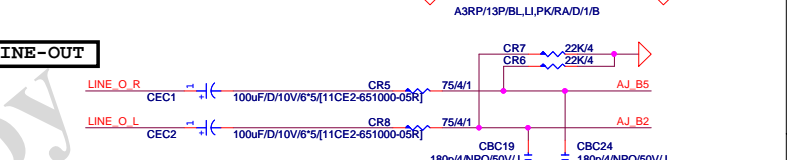
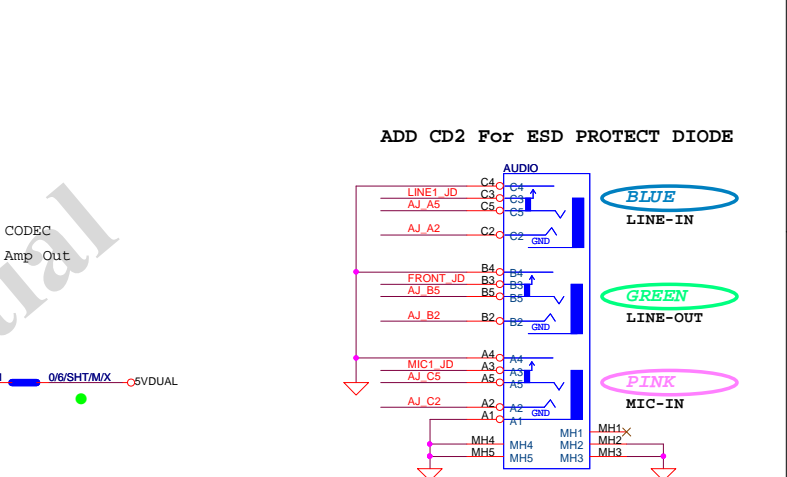
AZALIA CODEC ALC887-VD2/ALC889/VT1708S/VT1708SCE Colay

	ALC887-VD2	ALC889	VT1708S	VT1708SCE
CR65	X	O	O	X
CR64	X	X	X	O
CR44/CBC26	47ohm+1nF	47ohm+1nF	22ohm+100P	22ohm+100P
CR34	20K/1%	20K/1%	5.1K/1%	20K/1%
CR31	O	O	O	O
CR30	X	X	X	X
CBC1/CBC2	22uF/X5R	22uF/X5R	22uF/X5R	22uF/X5R
CR20	5.11K/4/1	5.11K/4/1	5.1K/4/1	5.1K/4/1
CBC35	O	X	X	O
CBC39/CBC40	N/A	N/A	100P/4	100P/4
CR6/CR7/CR54/CR58	22K/4	22K/4	10K/4	10K/4
CR5/CR8/CR13/CR11/CR57/CR53	75 ohm	62 ohm	75 ohm	75 ohm
CR51/CD1/CBC7	O	X	X	O
CD2/CD3/CQ3/CQ5	X	O	O	X
CR1/CR14/CR17/CR22	75 ohm	62 ohm	1K ohm	1K ohm

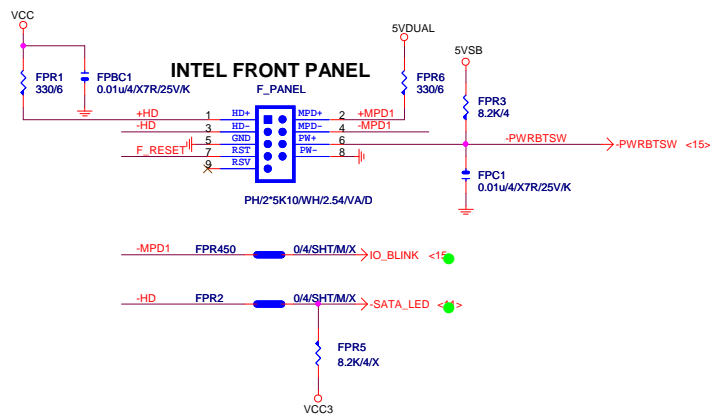
CODEC POWER/EMI PAD



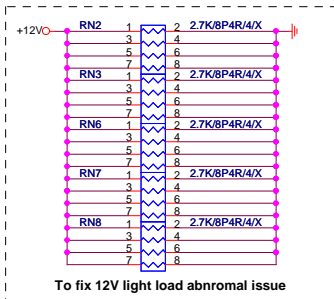
ADD CD2 For ESD PROTECT DIODE



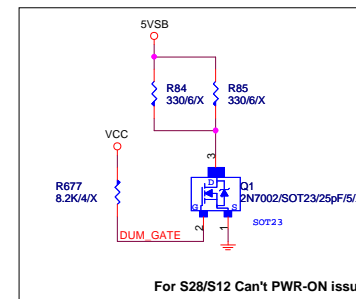
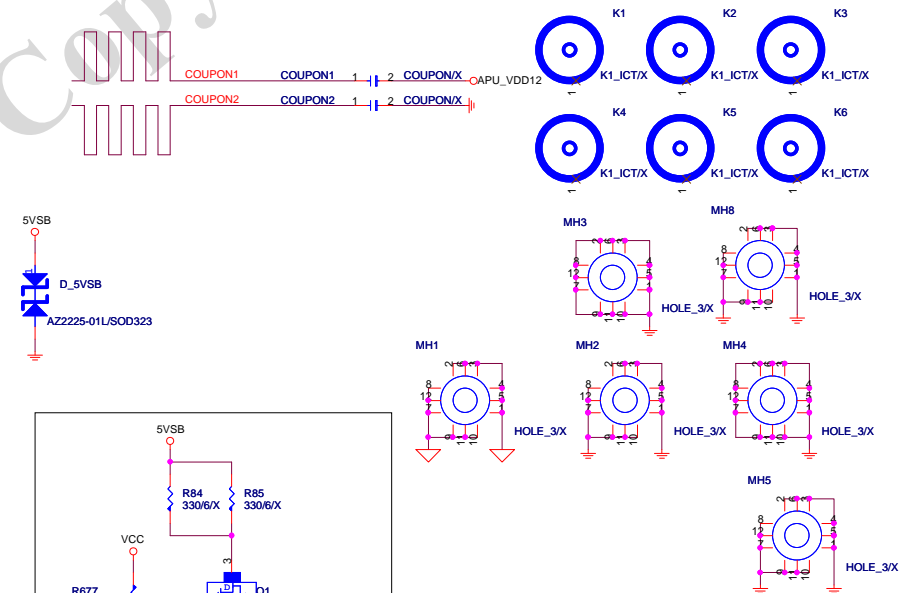
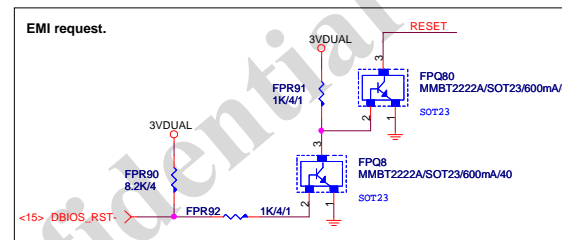
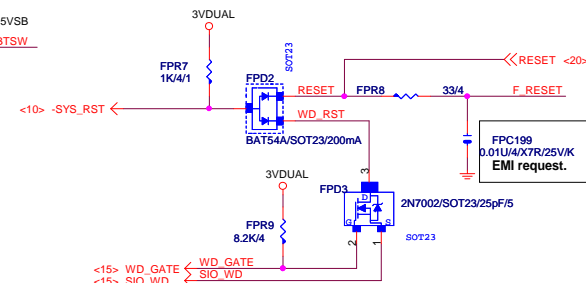
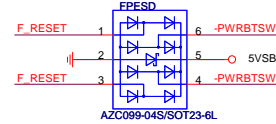
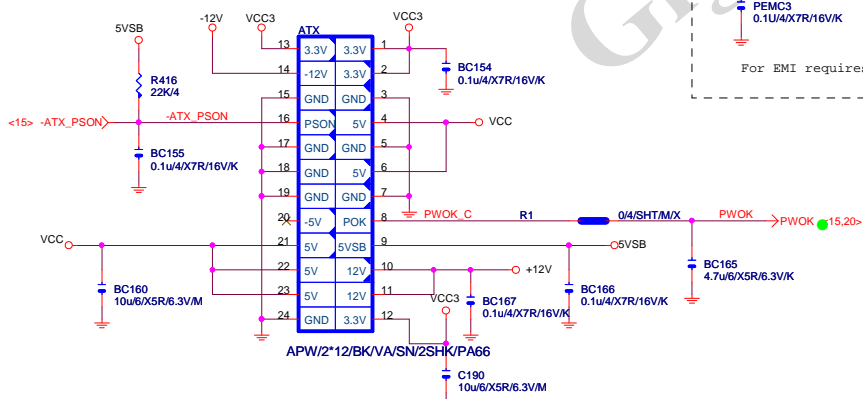
**GIGABYTE**  
Title: **HD AUDIO ALC887-VD2**  
Size: Custom Document Number: **GA-F2A68HM-DS2** Rev: **1.01**  
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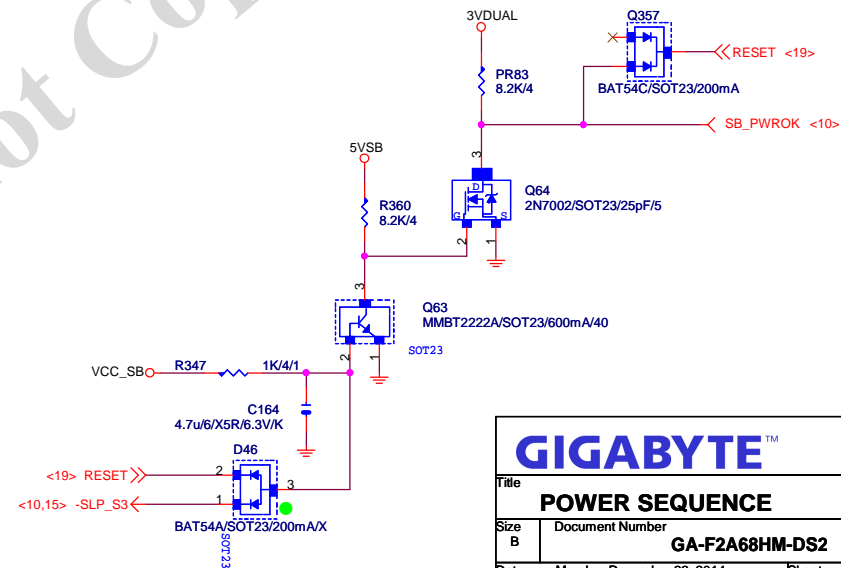
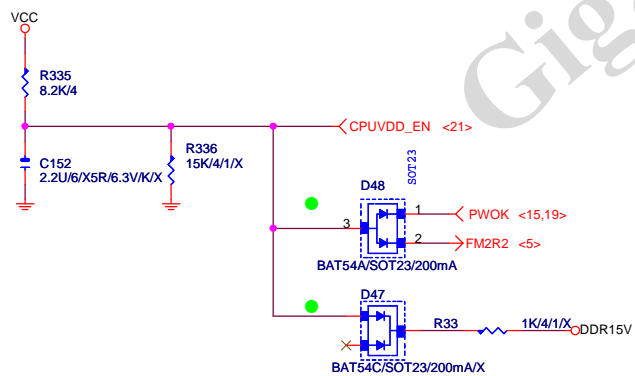
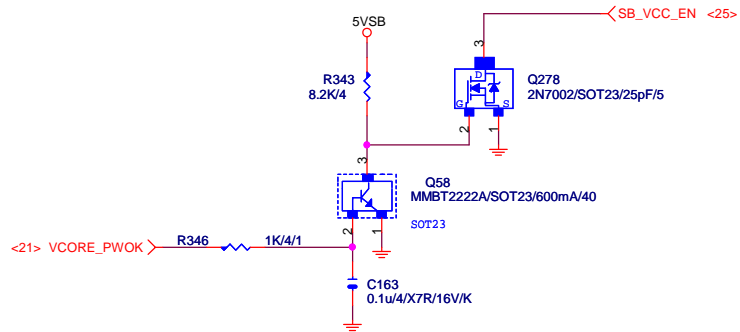


**ATX POWER CONNECTOR**



**GIGABYTE**

Title		
ATX, FRONT PANEL		
Size	Document Number	Rev
Custom	GA-F2A68HM-DS2	1.01
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**GIGABYTE™**

Title **POWER SEQUENCE**

Size B Document Number

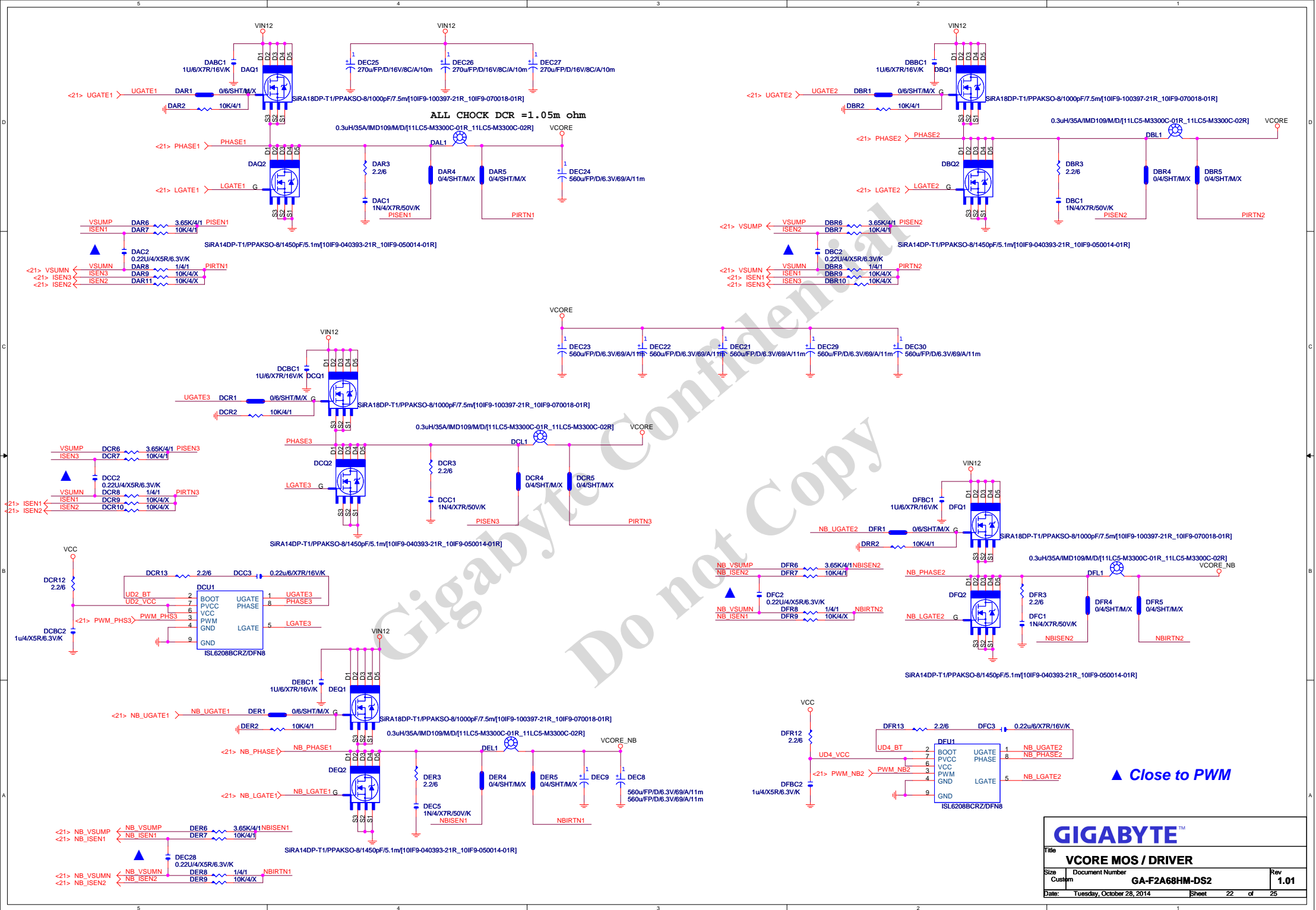
**GA-F2A68HM-DS2**

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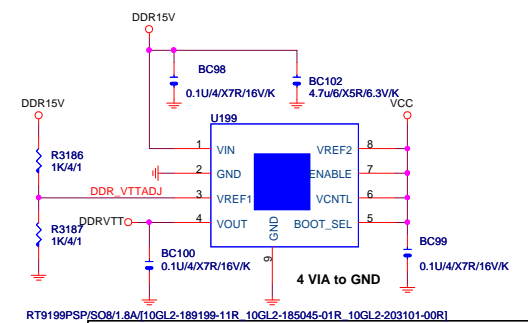
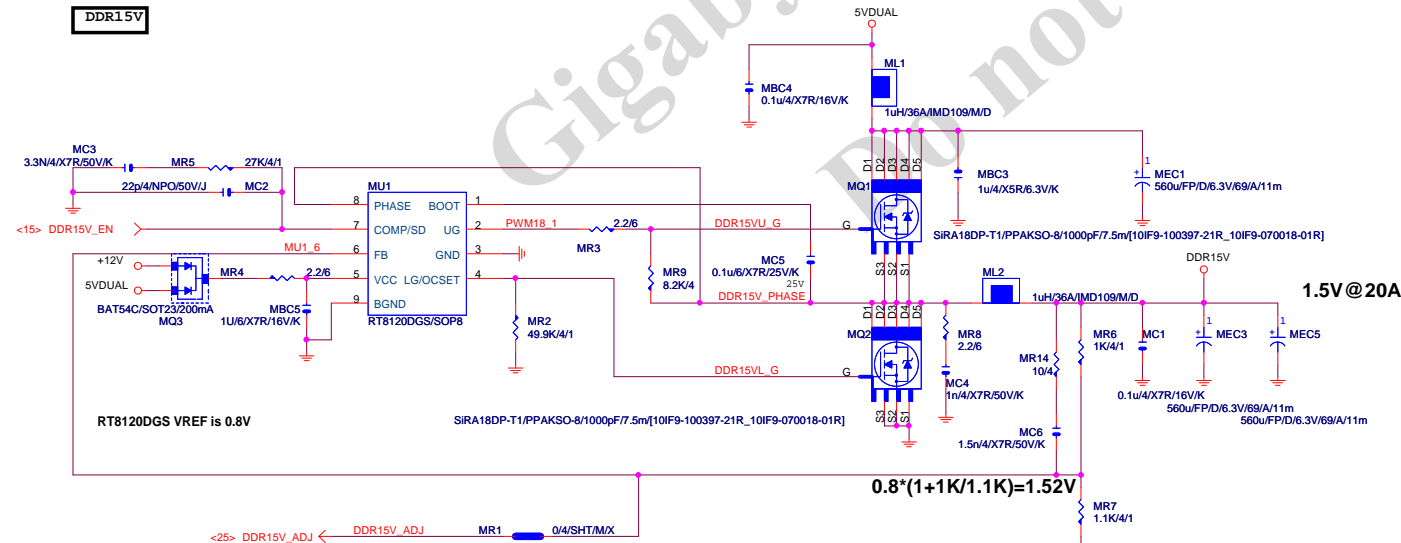
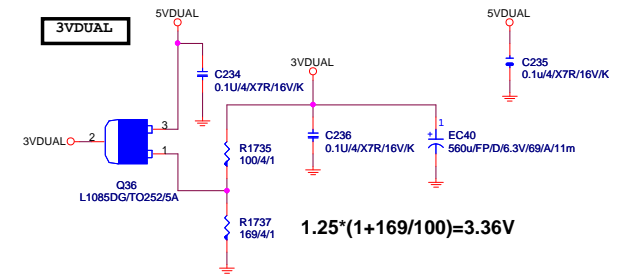
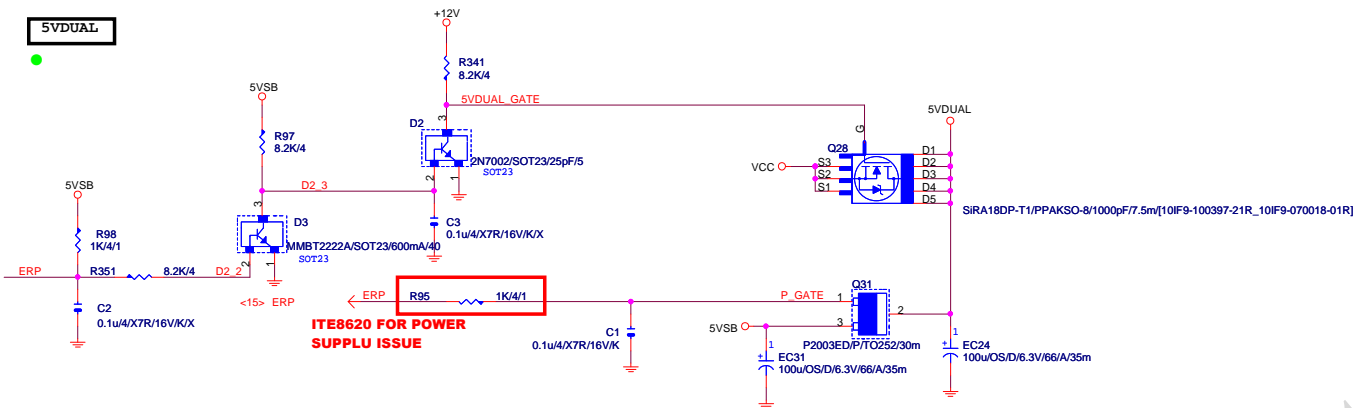
Date: Monday, December 22, 2014

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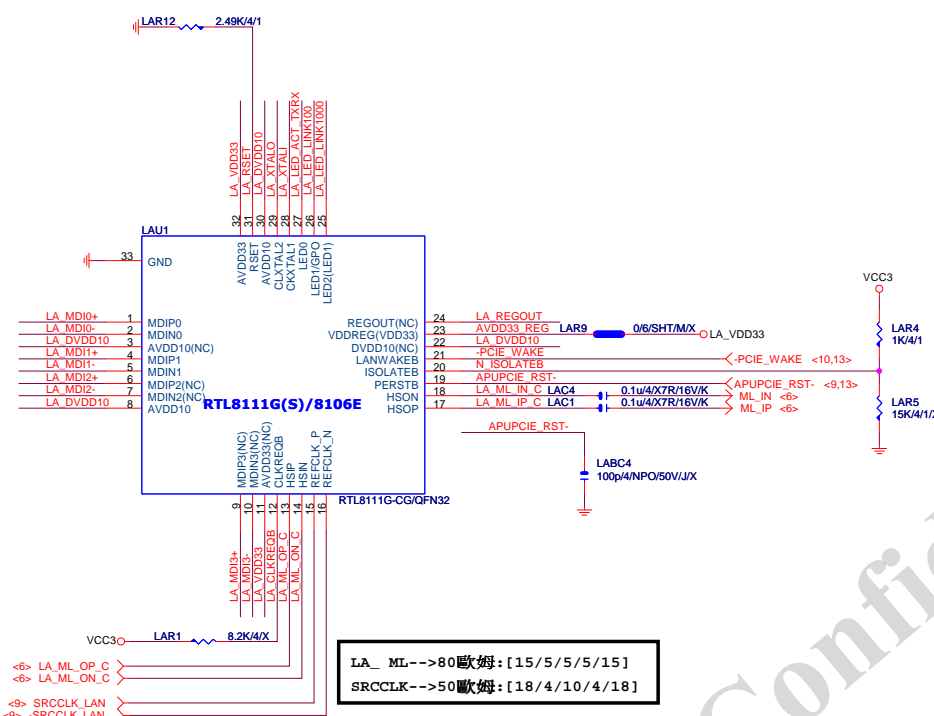
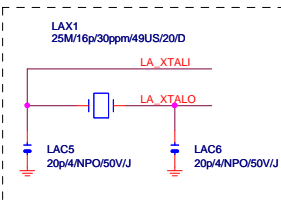




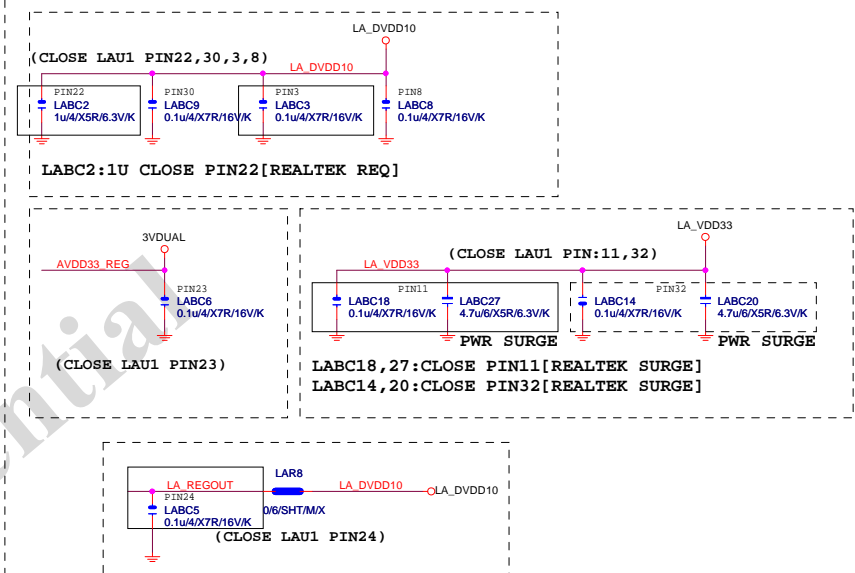
GIGABYTE™			
Title			
VCORE MOS / DRIVER			
Size	Document Number	Rev	
Custom	GA-F2A68HM-DS2	1.01	
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# LAN:RTL8111G

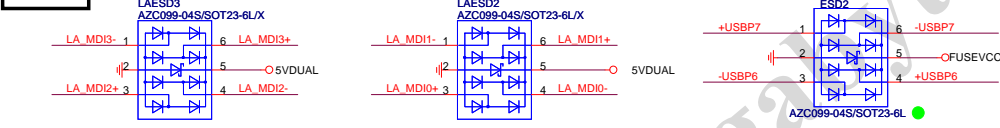


# LAN POWER



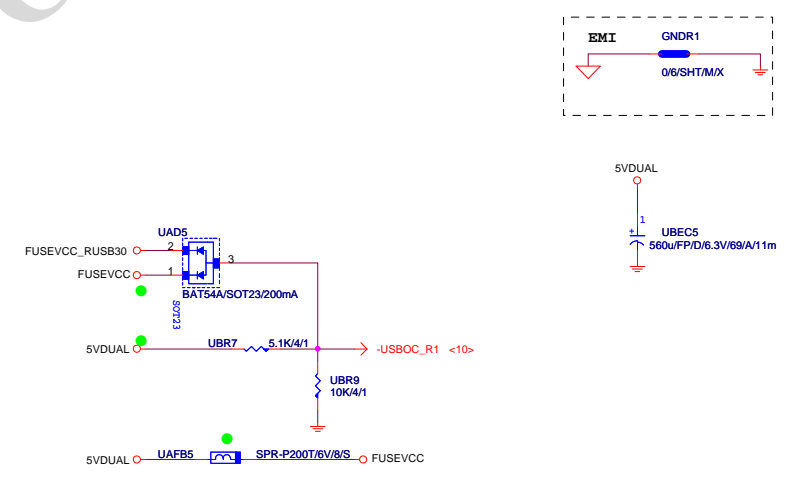
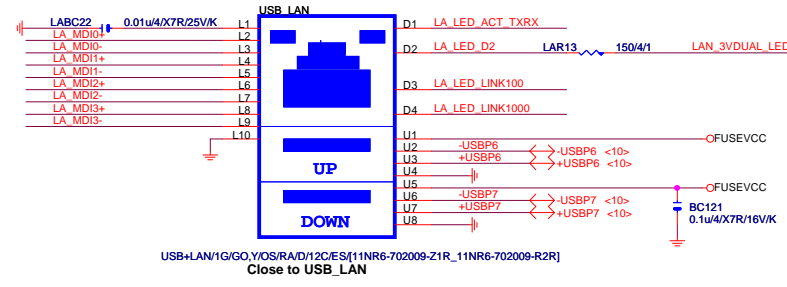
NOTE:  
RT8106E:PIN3,11,22,24-->NC  
LABC2LABC3,LABC5,LABC18,LABC27-->N/A

# USB\_LAN



LAN 100 Ohm  
USB 90 Ohm

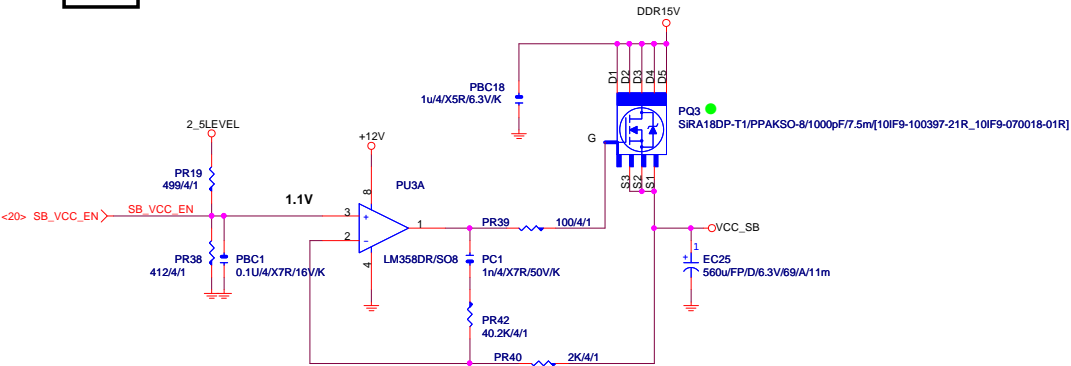
# USB\_LAN CONNECTOR



GIGABYTE™		
Title	REALTK RTL8111G	
Size	Document Number	Rev
Custom	GA-F2A68HM-DS2	1.01
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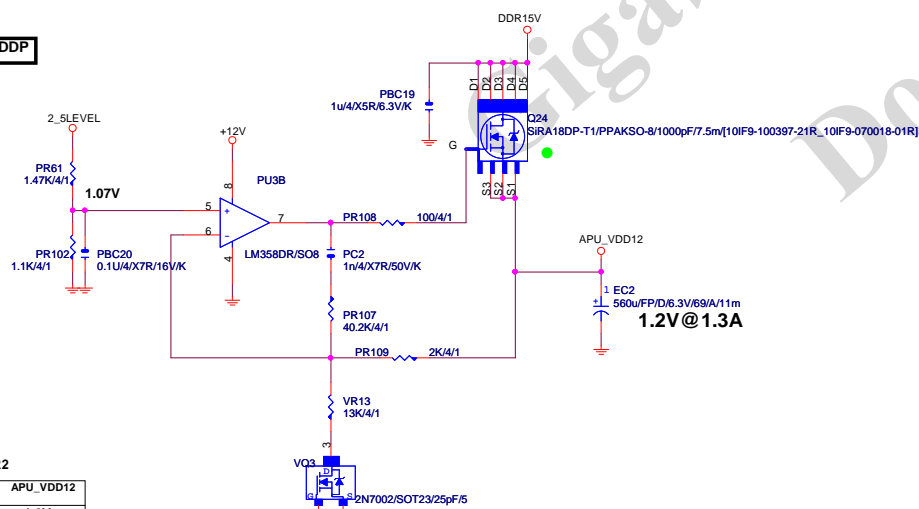


# VCC\_SB



2\_5LEVEL  
BC0  
22u/8/X5R/6.3V/M  
Near PR19 / PR61

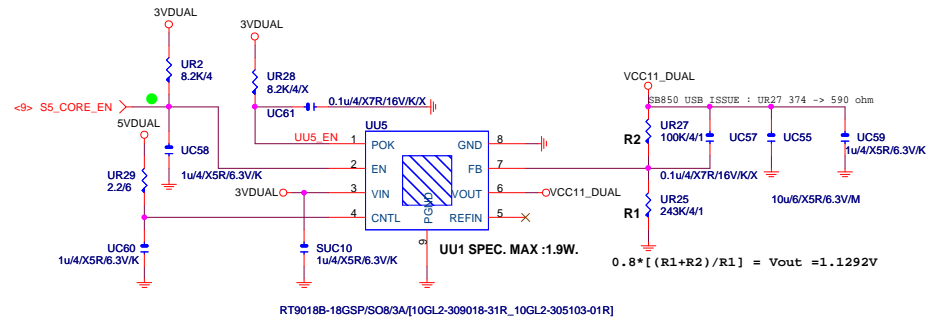
# APU\_VDDP



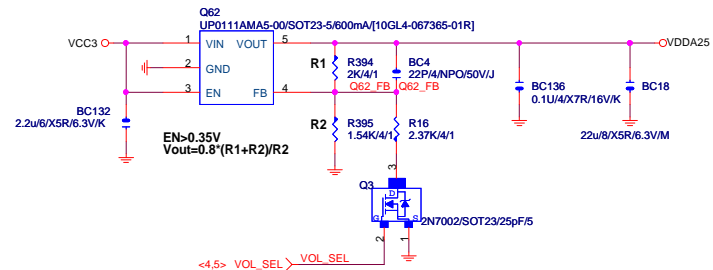
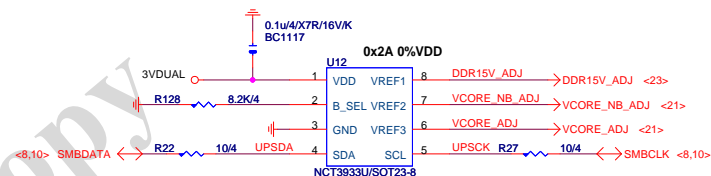
$$V_{out} = 1.07 \cdot (R1 + R2) / R2$$

APU	VOL_SEL	APU_VDD12
FM2	1	1.2V
FM2+	0	1.05V

<4,5> VOL\_SEL < VOL\_SEL



【技術通報R&D技術通報156】  
RT9018 (RICHTEK) 與 NCT3730 (NUVOTON),  
EM5103GE (EMC) 做共用, 針對 PIN7 (FB) 分壓阻值部份  
(R1/R2) 須做修改為 100K 以上電阻值



APU	VOL_SEL	VDDA25
FM2	1	2.5V
FM2+	0	1.8V

GIGABYTE

Title	VCC_SB, APU_VDDP, VCC11_DUAL, VDDA25
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